In the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-8. (Cancelled).

9. (Previously Presented) A method of fabricating a transistor, comprising:

forming a nitride-based channel layer on a substrate;

forming a barrier layer on the nitride-based channel layer;

forming a contact recess in the barrier layer to expose a contact region of the nitride-based channel layer;

forming a contact layer on the exposed contact region of the nitride-based channel layer using a low temperature deposition process;

forming an ohmic contact on the contact layer;

forming a gate contact disposed on the barrier layer adjacent the ohmic contact;

forming a first dielectric layer on the barrier layer;

forming a gate recess in the first dielectric layer;

wherein forming a gate contact comprises forming a gate contact in the gate recess; and

wherein forming a contact recess comprises forming an ohmic contact recess in the first dielectric layer and the barrier layer that expose a portion of the nitride-based channel layer.

10. (Original) The method of Claim 9, wherein the first dielectric layer comprises a silicon nitride layer.

11. (Original) The method of Claim 10, wherein the silicon nitride layer provides a passivation layer for the transistor.

12. (Previously Presented) A method of fabricating a transistor, comprising:

forming a nitride-based channel layer on a substrate;

forming a barrier layer on the nitride-based channel layer;

forming a contact recess in the barrier layer to expose a contact region of the nitride-based channel layer;

forming a contact layer on the exposed contact region of the nitride-based channel layer using a low temperature deposition process;

forming an ohmic contact on the contact layer;

forming a gate contact disposed on the barrier layer adjacent the ohmic contact;

forming a first dielectric layer on the barrier layer;

wherein forming a gate contact comprises forming a gate contact in the first dielectric layer; and

wherein forming a contact recess comprises forming an ohmic contact recess in the first dielectric layer and the barrier layer that expose a portion of the nitride-based channel layer.

13-21. (Cancelled).

22. (Previously Presented) A method of fabricating a transistor, comprising:

forming a nitride-based channel layer on a substrate;

forming a barrier layer on the nitride-based channel layer;

forming a contact recess in the barrier layer to expose a contact region of the nitride-based channel layer;

forming a contact layer on the exposed contact region of the nitride-based channel layer using a low temperature deposition process;

forming an ohmic contact on the contact layer;

forming a gate contact disposed on the barrier layer adjacent the ohmic contact;

forming holes in the channel layer adjacent the contact regions;

placing n-type nitride-based semiconductor material in the holes; and

wherein forming an ohmic contact on the contact layer comprises forming an ohmic contact on the contact layer and on the n-type nitride-based semiconductor material in the holes.

23-24. (Cancelled).

25. (Previously Presented) A method of fabricating a transistor, comprising:

forming a nitride-based channel layer on a substrate;

forming a barrier layer on the nitride-based channel layer;

forming a masking layer on the barrier layer;

patterning the masking layer and the barrier layer to provide a contact opening that exposes a portion of the nitride-based channel layer;

forming a contact layer on the exposed portion of the nitride-based channel layer and the masking layer;

selectively removing the masking layer and a portion of the contact layer on the masking layer to provide a nitride-based contact region;

forming an ohmic contact on the nitride-based contact region; and

forming a gate contact disposed on the barrier layer adjacent the ohmic contact.

26. (Original) The method of Claim 25, further comprising:

forming a first dielectric layer on the barrier layer;

forming a recess in the first dielectric layer;

wherein forming a gate contact comprises forming a gate contact in the recess;

wherein forming a masking layer on the barrier layer comprises forming a masking layer on the first dielectric layer; and

wherein patterning the masking layer and the barrier layer to provide a contact opening that exposes a portion of the nitride-based channel layer comprises patterning the masking layer, the first dielectric layer and the barrier layer to provide a contact opening that exposes a portion of the nitride-based channel layer.

27. (Original) The method of Claim 25, wherein the first dielectric layer comprises a silicon nitride layer.

28. (Original) The method of Claim 27, wherein the silicon nitride layer provides a passivation layer for the transistor.

29. (Original) The method of Claim 25, wherein the masking layer comprises a dielectric layer.

30. (Original) The method of Claim 29, wherein the dielectric layer comprises a silicon oxide layer.

31. (Original) The method of Claim 25, wherein the masking layer comprises a photoresist and/or e-beam resist masking layer.

32. (Original) The method of Claim 25, wherein forming an ohmic contact comprises forming an ohmic contact without annealing the ohmic contact.

33. (Original) The method of Claim 25, wherein forming an ohmic contact comprises:

patterning a metal layer on the nitride-based contact region; and

annealing the patterned metal layer at a temperature of less than about 850 °C.

34. (Previously Presented) The method of Claim 25, wherein forming a nitride based contact layer on the exposed portion of the nitride-based channel layer and the masking layer comprises forming a nitride based contact layer by metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), plasma enchanced chemical vapor deposition (PECVD), sputtering and/or hydride vapor phase epitaxy (HVPE).

35. (Previously Presented) The method of Claim 25, wherein forming a nitride based contact layer on the exposed portion of the nitride-based channel layer and the masking layer comprises forming a nitride based contact layer on the exposed portions of the nitride-based channel layer and the masking layer to a thickness sufficient to provide a sheet resistivity of less than a sheet resistivity of a two-dimensional electron gas region formed at an interface between the channel layer and the barrier layer.

36. (Previously Presented) The method of Claim 25, wherein forming a nitride based contact layer comprises forming n-type an InGaN, GaN, AlGaN, InAlGaN, InAlN and/or InN layer.

37. (Previously Presented) The method of Claim 36, wherein the InGaN, GaN, AlGaN, InAlGaN, InAlN and/or InN layer is doped with Si, Ge and/or O during formation.

38. (Previously Presented) The method of Claim 25, wherein the nitride based contact layer comprises an n-type degenerate semiconductor material other than GaN and AlGaN.

39. (Previously Presented) The method of Claim 38, wherein the nitride based contact layer comprises a non-nitride Group III-V semiconductor material, a Group IV semiconductor material and/or a group II-VI semiconductor material.

40. (Previously Presented) The method of Claim 25, further comprising forming sidewalls of the channel layer to provide an increased surface area interface between the nitride based channel layer and the nitride based contact layer in comparison to a planar interface.

41. (Original) The method of Claim 40, wherein forming an ohmic contact comprises forming an ohmic contact on the nitride-based contact region that extends onto a portion of the channel layer.

42. (Original) The method of Claim 40, wherein forming an ohmic contact comprises forming an ohmic contact on the nitride-based contact region that terminates before the sidewall of the channel layer.

43. (Previously Presented) The method of Claim 25, further comprising:

forming holes in the channel layer adjacent the nitride-based contact region;

wherein forming a nitride based contact layer further comprises placing a nitride-based semiconductor material in the holes; and

wherein forming an ohmic contact on the nitride-based contact region comprises forming an ohmic contact on the nitride-based contact region and on the nitride-based semiconductor material in the holes.

44. (Previously Presented) The method of Claim 25, wherein the contact opening comprises a first contact opening, the nitride-based contact region comprises a first nitride-based contact region and the ohmic contact comprises a first ohmic contact, the method further comprising:

patterning the masking layer and the barrier layer to provide a second contact opening that exposes a portion of the nitride-based channel layer;

forming a nitride based contact layer on the portion of the nitride-based channel layer exposed by the second contact opening;

wherein selectively removing the masking layer comprises selectively removing the masking layer and a portion of the nitride based contact layer on the masking layer to provide the first nitride-based contact region and a second nitride-based contact region;

forming a second ohmic contact on the second nitride-based contact region; and

wherein forming a gate contact comprises forming a gate contact disposed on the barrier layer between the first and second ohmic contacts.

45. (Previously Presented) The method of Claim 25, further comprising a contact recess that exposes a portion of the barrier layer and wherein forming a nitride based contact layer comprises forming a contact layer that extends onto the exposed portion of the barrier layer.

46-84. (Cancelled).